Design and Characterization of Submicron CCDs in CMOS

Keith Fife, Abbas El Gamal and H.-S. Philip Wong
Department of Electrical Engineering, Stanford University, Stanford, CA 94305
Phone: 650-725-9696, Fax: 650-724-3648, E-mail: kfife@stanford.edu

Abstract

Three types of submicron CCDs are implemented in single-poly 0.11μm CMOS technology to demonstrate the feasibility of multi-aperture imaging systems that produce data from distributed arrays of CCDs integrated across a monolithic substrate. Test structures comprising 16×16 pixel Frame-Transfer (FT)-CCDs with $0.5-0.7\mu$m pixels are fabricated under various process conditions to implement devices which operate as surface-channel, buried-channel and pinned phase buried-channel. Ripple charge transfer and single electrode charge confinement are implemented to minimize pixel pitch.

Introduction

As pixel size is approaching the limits of conventional optics, improvements in resolution are diminishing. Scaling pixels beyond these limits, however, can provide new imaging capabilities beyond merely attempting to increase spatial resolution. In [1], we describe a multi-aperture approach to imaging, whereby the image sensor is partitioned into an array of apertures, each with its own local subarray of pixels and image-forming optics. A virtual image is focused a certain distance above the sensor such that the apertures capture overlapping views of the scene. The subimages are post-processed to obtain both a high resolution 2D image and a depth map. A key feature of this design is in the use of submicron pixels to obtain accurate depth measurements derived from the localization of features within adjacent subarrays.

This paper presents the design and characterization of 3 types of CCD structures implemented in 0.11μm CMOS technology: surface-channel, buried-channel, and pinned phase buried-channel. Each CCD structure differs in the location of charge storage during the integration time and in the sequencing of the electrodes during charge transfer. Our surface-channel design was reported in [2]. We used the buried-channel CCD design in a multi-aperture image sensor reported in [3]. A new pinned phase buried-channel design is implemented to improve dark current and charge transfer efficiency.

Design, Fabrication, and Operation

We use an FT-CCD architecture to minimize pixel pitch and to eliminate metal layers in the active imaging area. Each test structure consists of a pixel array, a storage array, a horizontal (H)-CCD, and a source follower readout circuit (see Fig. 1). The storage array is covered by metal layers that are also used to distribute global control lines (see Fig. 2). A photomicrograph is shown in Fig. 3. Each pixel consists of a single poly electrode, a channel, and a channel stop. The channels and stops are shown in Fig. 4. The electrodes are patterned with non-silicided polysilicon as shown in Fig. 5. Each pixel array is separated by a wall of 4 metal layers. The first 2 metal layers are shown in Fig. 6.

In all designs, the polysilicon is doped by masking out the channels as shown in Fig. 7. The polysilicon for the surface-channel device is doped N+ and the buried-channel designs are doped P+ to shift the workfunction closer to the operating range of CMOS circuits. The IOs on the test chip were designed to allow both positive and negative voltage sequencing. SEM images for each cross section of the surface-channel device are shown in Fig. 8 and Fig. 9. Electrode spacing of 180nm was used in all designs. The polysilicon is 130nm thick with gate oxide of 8nm. The channel stop for the surface-channel device is STI. The channel stop for the buried-channel is formed by a p-type implant (BF2, 75keV, 4.0E13/cm^2). The SEM for the H-CCD with fill-and-spill input and floating diffusion is shown in Fig. 10. The required sequencing for this design is described in [3].

The pinned phase buried-channel design is shown in Fig. 11 with doping profiles plotted in Fig. 12-13. This design is similar to the open-pinned phase CCD described in [4] where the channel is inverted during the integration time. Instead of integrating charge under the p-type implant, we integrate charge under the electrode with an inverted surface. During the integration time, the entire surface is pinned with a large concentration of holes provided by the channel stops, which reduces the dark current at the interface.

An image is captured by integrating photocharge at each electrode or at every other electrode for higher well capacity. The integration begins by depleting the CCDs of charge via transfer to the upper diffusion V0. During integration, the pixel array electrodes are held at an intermediate voltage. At the end of integration, the accumulated charge is ripple transferred row-by-row to the storage array and then into the H-CCD one pixel at a time until every pixel has been double sampled at the floating diffusion and buffered by the source follower transistor.

Simulation and Measurement Results

Simulated potential diagrams along the channel (wherever the max potential occurs) for several phases are shown for all 3 designs in Fig. 14-16. Single electrode charge confinement is achieved in the surface-channel device due to the barriers created by the poly gap spacing, whereas it is achieved in the buried-channel device due to the induced pockets. The pinned phase design uses the self-aligned p-type implants as barriers to confine the charge. Although the surface potential is pinned to the channel stop potential, the depleted channel under the electrode remains at a higher potential. With sufficient gate voltage, each of the designs overcomes the pocket or barrier that creates the confinement and charge is transfered away from one region and then packed again at single electrode pitch into another.

Charge transfer efficency (CTE) is measured the highest for the surface-channel device at just above 99.9%. We also fabricated the surface-channel device with p-type channel stops and found that the CTE degrades. When the surface channel electrodes are first accumulated with holes, the CTE drops to as low as 85% whereas the buried-channel devices don't degrade under this condition. The conversion gain for the 0.5 μm pixel is 193μV/e- and 165μV/e- for the 0.7 μm pixel. There is no significant difference between the 3 types of CCDs because the readout transistors are identical. Despite the use of poly electrodes, the QE is reasonable for short wavelengths as shown in Fig. 18. This is due to the thin the poly layer and the open space in between each electrode. The dark current is about 35e-/sec for both the surface and buried-channel devices (See Fig. 19). The dark current improves by a factor of 15 for the pinned phase device.

References

[1] K. Fife, A. El Gamal, and H. Wong, "A 3D multi-aperture image sensor architecture," *Custom Integrated Circuits Conference*, pp. 281–284, Sep. 2006.

[2] ——, "A 0.5μm pixel frame-transfer CCD image sensor in 110nm CMOS," *IEDM*, pp. 1003–1006, Dec. 2007.

[3] ——, "A multi-aperture image sensor with 0.7μm pixels in 0.11μm CMOS technology," *IEEE J. Solid-State Circuits*, pp. 2990–3005, Dec. 2008.

[4] J. Janesick, "Open-pinned phase CCD technology," *Proc.SPIE 1159*, 1989.

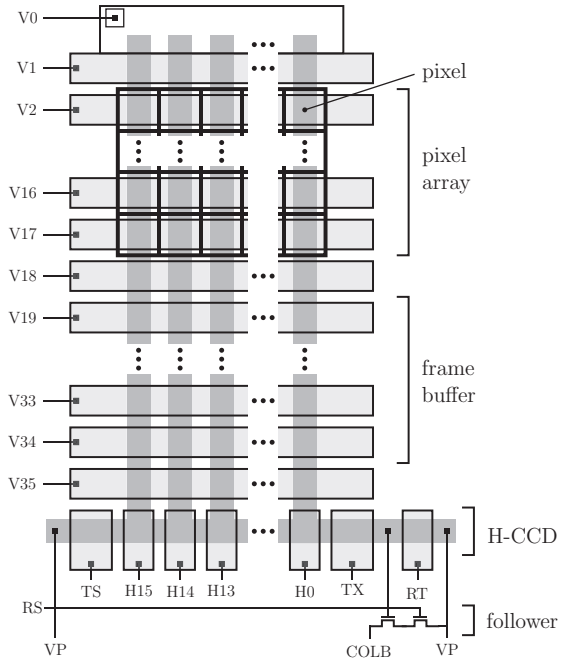

Fig. 1. FT-CCD schematic showing the pixel array, frame buffer, H-CCD and follower readout.

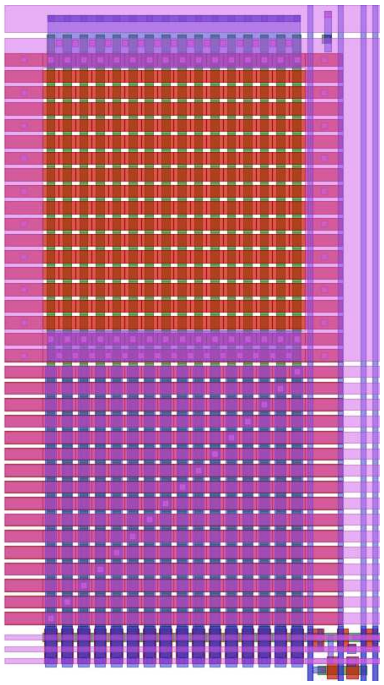

Fig. 2. CAD layout of the 16×16 FT-CCD.

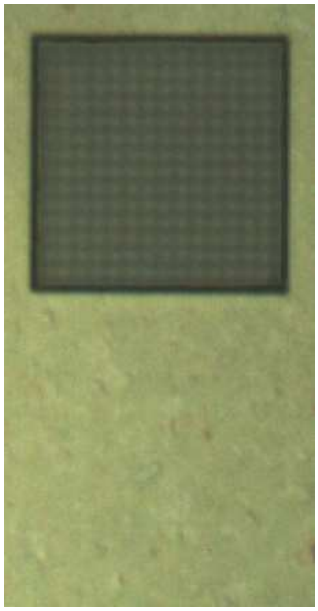

Fig. 3. Photomicrograph of a fabricated 16×16 FT-CCD. Two photos are combined to simultaneously focus on the pixels and the top metal.

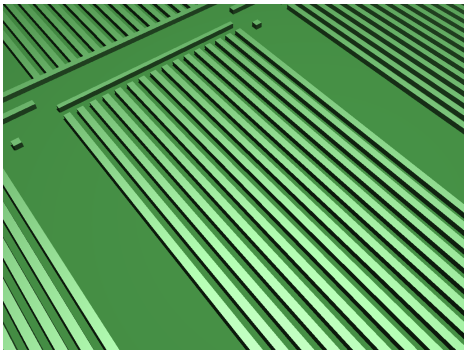

Fig. 4. Channel and channel stops for the FT-CCD.

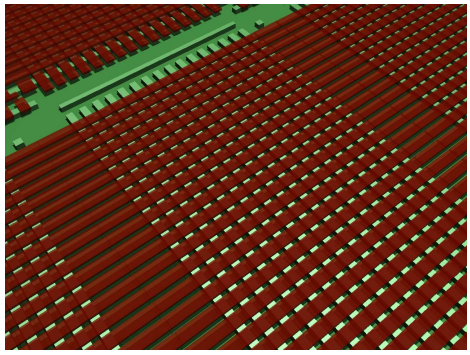

Fig. 5. Placement of the polysilicon electrodes.

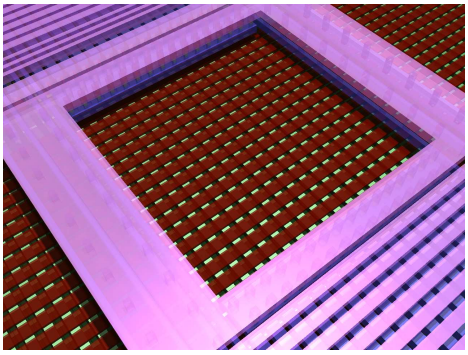

Fig. 6. Metal routing and isolation between arrays.

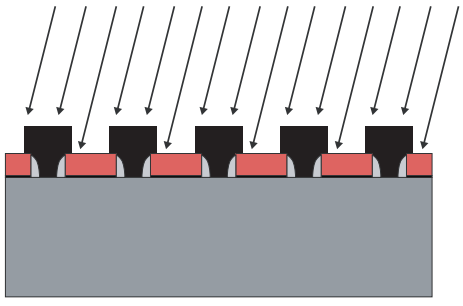

Fig. 7. Method for doping the polysilicon such that the channel region is protected.

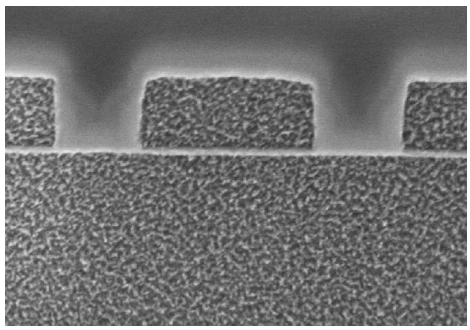

Fig. 8. Cross-section of the surface-channel CCD along the channel.

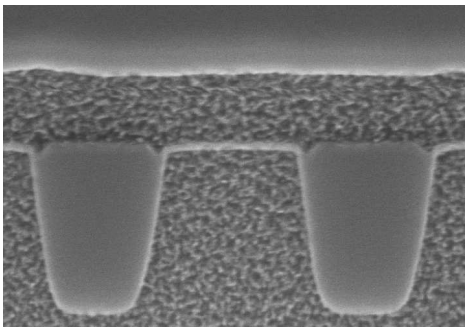

Fig. 9. Cross-section of the surface-channel CCD against the channel stops.

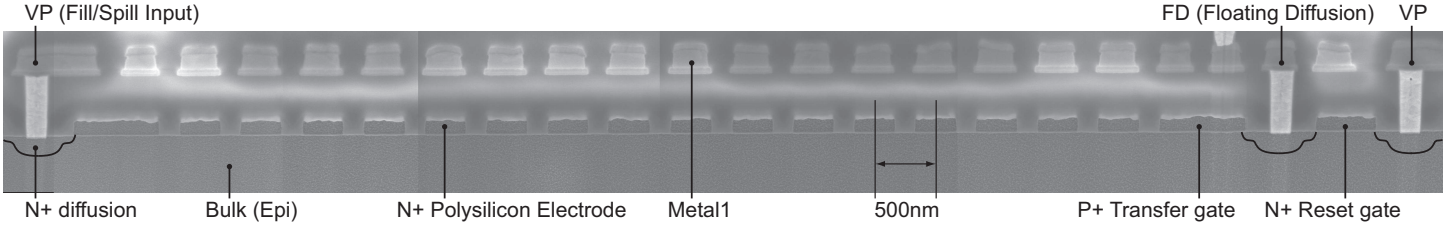

Fig. 10. SEM of 16-stage H-CCD showing fill/spill input for electrical testing, floating diffusion for output charge-to-voltage conversion, and the reset gate.

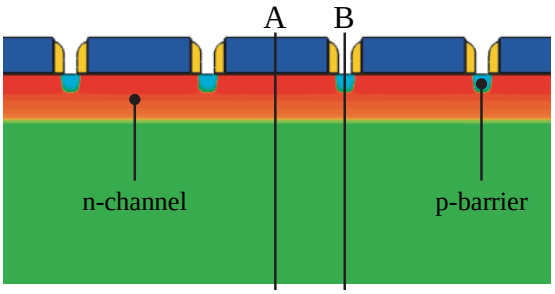

Fig. 11. Design of the pinned phase buried-channel CCD showing P+ electrodes with n-type channel against section A and self-aligned p-type barriers against section B.

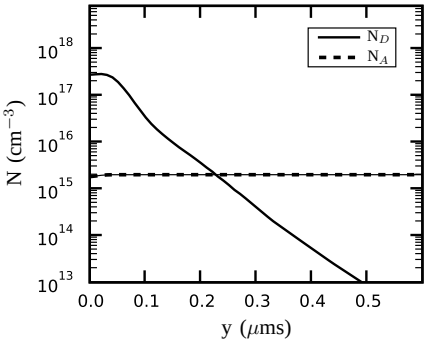

Fig. 12. Simulated doping profile along cross-section A.

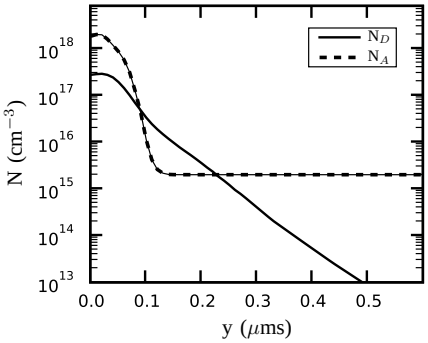

Fig. 13. Simulated doping profile along cross-section B.

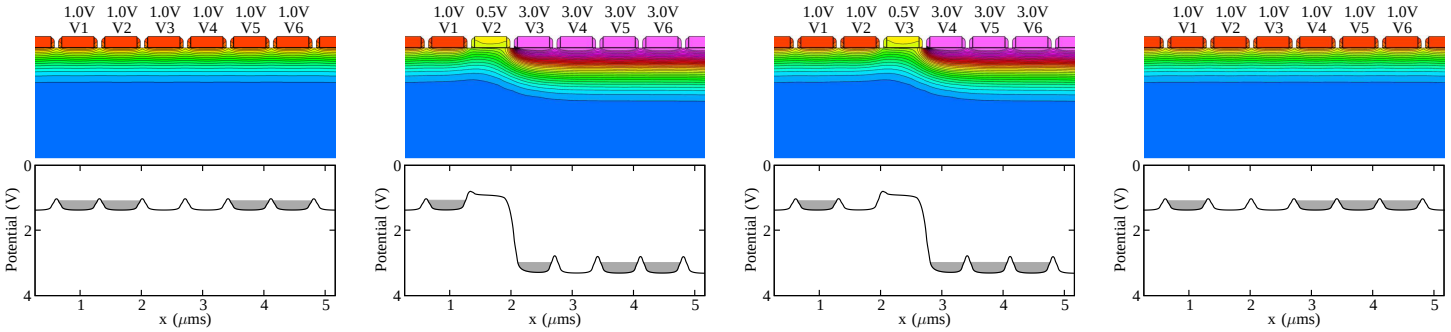

Fig. 14. Potential diagrams for the surface-channel CCDs with single electrode charge confinement during ripple charge transfer.

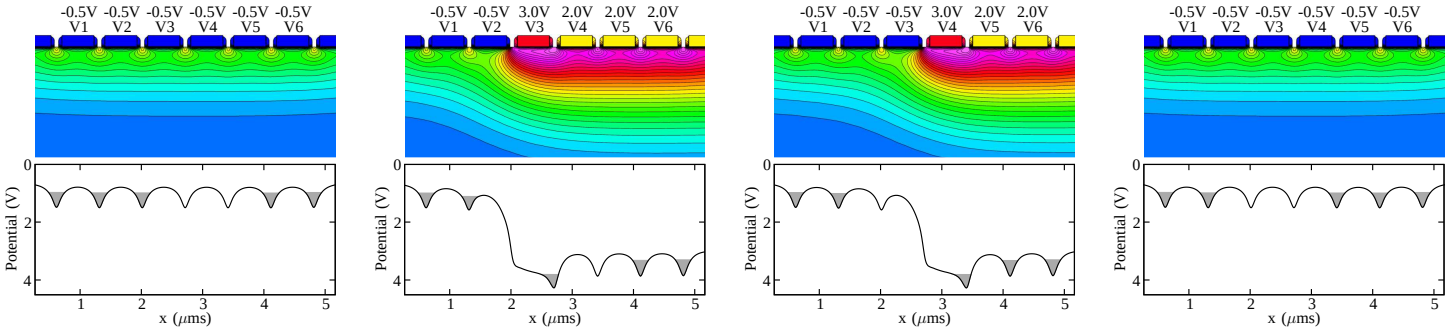

Fig. 15. Potential diagrams for the buried-channel CCDs with single electrode charge confinement during ripple charge transfer.

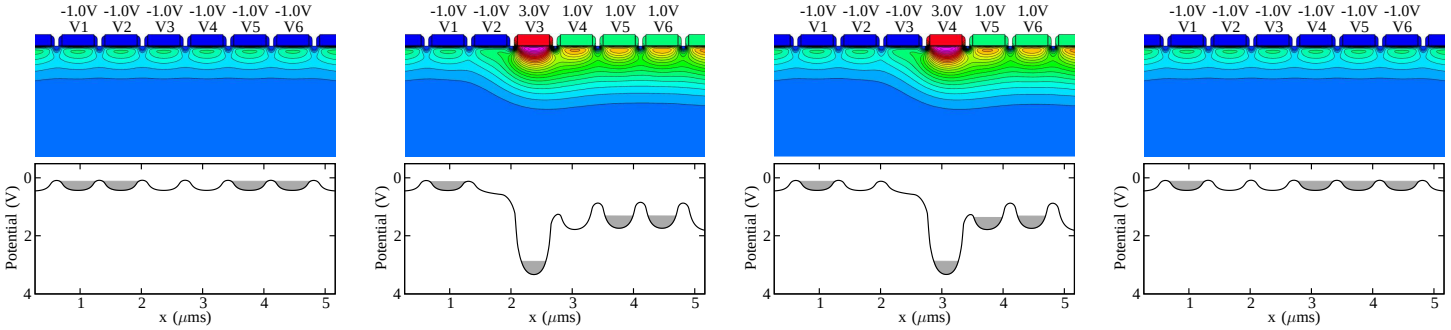

Fig. 16. Potential diagrams for the pinned phase buried-channel CCDs with single electrode charge confinement during ripple charge transfer.

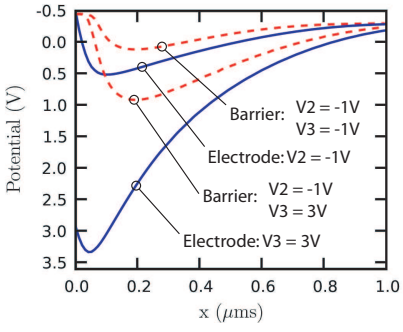

Fig. 17. Pinned phase diagram showing the barrier potentials relative to the potentials under the electrode region at separate phases.

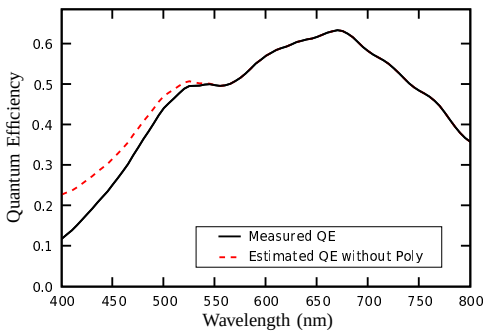

Fig. 18. Measured QE for the buried-channel CCD.

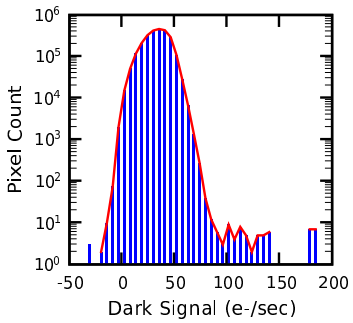

Fig. 19. Dark signal distribution for the buried-channel CCD at RT.